**VLSI**

1. VLSI Sub-System design: Multiplexers, Adders, Shift Registers
2. MOS transistor: Linear non-linear operation, MOS Capacitance, Thermal noise and leakage current.
3. CMOS scaling and ITRS roadmap
4. CMOS inverter circuits and system design
5. Logic family
6. What is the number gates per chip in the VLSI integrated circuit?
7. 100-1000
8. 1000-20000
9. >20000
10. Multiple Ips
11. According to the ITRS roadmap, what was the feature size for metal oxide semiconductor in 2010s?
12. 65nm
13. 45nm
14. 22nm
15. 10nm
16. What is the number of NOR gate required in the gate level design of the 1-bit full adder circuit?
17. 0
18. 1
19. 2
20. 3
21. In Y-chart representation of VLSI design flow, which one of these parameters does not fall in the structural domain?
22. Processor
23. Leaf cell
24. Register ALU
25. Cell placement
26. Functions and interfaces of various functional blocks of a larger system should follow the concept of…
27. Modularity
28. Locality
29. Regularity
30. Stability
31. For Si, of intrinsic concentration is and hole mobile carrier concentration is , then the electron mobile carrier concentration is?
32. The affinity of a material is defined as the difference between the
33. Fermi level and valance band
34. Fermi level and free space
35. Free space and conduction band
36. Free space and intrinsic fermi level
37. If at zero gate bias voltage, no conducting channel region is present, than the operating mode of MOS transistor is called as…
38. Mixed mode
39. Cut-off mode
40. Enhancement mode
41. Depletion mode
42. If the acceptor concentration MOS transistor is increased, then the threshold voltage will...
43. Increase
44. Decrease
45. Independent of the acceptor quantity
46. Null effect
47. If , and , then what the fermi potential for p-type substrate?
48. -0.55V
49. 0.51V
50. -0.51V
51. 0.55V
52. The pinch-off points occur at.
54. If , , , and , than determine the parameter =?
55. 1.68
56. 2.38
57. 3.00
58. 3.20
59. If S is the scaling parameter, then in full scaling of MOSFET, the gate oxide thickness is..
60. Increased by parameter S
61. Decreased by parameter S
62. Increased by parameter
63. Decreased by parameter
64. Due to channel length modulation, the length of the channel is
65. Shortened
66. Extended
67. Constant
68. Can be any of the above
69. For CMOS gate array process, what is the minimum feature size (in µm) in 45nm technology scale?
70. 1.00
71. 0.80
72. 0.50
73. 0.35
74. SRAM stand for:
75. Simultaneous Read Arbitrary Memory
76. Slow Read Access Memory
77. Static Read Access Memory
78. Static Random-Access Memory
79. MOSFET is which type of device?
80. Current controlled
81. Voltage controlled current source
82. Voltage controlled
83. Voltage controlled voltage source
84. Which one is normally referred to as ON switches?
85. JFET
86. UJT
87. Depletion MOSFET
88. Enhancement MOSFET
89. For an n-channel MOSFET, if the conduction parameter (Kn) is 0.249 mA/V2, gate to source voltage VGS = 1.5V and VTH=0.75V. The current will be?
90. 0.160 mA
91. 0.150 mA
92. 0.140 mA
93. 0.130 mA
94. An NMOS has Id= 5 mA, VGS=2V, VDS=4V and VT=0.8V. if the thickness of oxide is 500 Ǻ, then the Aspect ratio of the device at the room temperature is?
95. 1.5
96. 14
97. 25
98. 35
99. Why is an N-channel MOSFET is preferred over a P-channel MOSFET?
100. Because of low noise
101. Because of low input impedance
102. Because it allows fast switching
103. Because of high gain factor
104. Which of the following mainly constitute the output capacitance?
105. Inter electrode capacitance
106. Stray capacitance
107. Junction parasitic capacitance
108. All of the above
109. The junction parasitic capacitance is produced due to \_\_\_\_
110. Source diffusion regions
111. Gate diffusion regions
112. Drain diffusion regions
113. All of the above
114. The amount of gate oxide capacitance is determined by\_\_\_
115. Charge present on the gate
116. Polarity of the gate
117. Charge present on the substrate
118. Area of the gate
119. Thermal noise in MOSFET is generated by \_\_\_
120. Conduction of the charge carriers in the channel
121. Electric field across the gate and channel
122. Capacitance of the gate oxide
123. Substrate bias effect
124. Thermal noise in MOSFET is proportion to:
125. Transconductance
126. Resistance
127. Gate voltage
128. None of the mentioned
129. In positive logic conversion for inverters, the condition for output voltage =VDD is:
130. Input voltage must be Zero
131. Input voltage between 0 to Vth.
132. Input voltage between Vth to VDD.
133. Input voltage must be VDD.
134. Larger input voltages which satisfy dVout/dVin = -1, are termed as:
135. VIL
136. VIH
137. VOL
138. VOH
139. The noise immunity of the circuit \_\_\_\_\_\_\_\_\_ with noise margin.
140. Incraeses
141. Decreases
142. Remains stable
143. Have no effect
144. The transition region has voltage range between\_\_
145. VOL to VIL
146. VIL to VIH
147. VIH to VOH
148. VOL to VOH